

ABSTRACT

A multi-processor computer architecture reduces processing time and bus bandwidth during snoop processing. The architecture includes processors and local caches. Each local cache corresponds to one of the processors. The architecture includes one or more virtual
5 busses coupled to the local caches and the processors, and one or more intermediary caches, where at least one intermediary cache is coupled to each virtual bus. Each intermediary cache includes a memory array and means for ensuring the intermediary cache is inclusive of associated local caches. The architecture further includes a main memory having a plurality of memory lines accessible by the processors.